High Speed Low Power Output Buffer amplifier for large-size LCD Applications

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ABSTRACT: The present paper Performance improvement in high speed low power out put Buffer amplifier for large –LCD applications. The proposed buffer achieves high-speed driving performance while drawing a low quiescent current during static operation. The circuit offers enhanced slewing capabilities with limited power consumption by exploiting a slew detector which monitors the output voltage of the input differential amplifier and outputs an additional current signal providing slew-rate enhancement at the output stage. Post-layout simulations show that the proposed buffer can drive a 1000pF column line load with 8.5-V/µs slew-rate and 0.6-µs settling time, while drawing only 8-µA static current from a 1.2 -V power supply.

I. INTRODUCTION

As the display resolution increases, the load capacitance of buffer amplifier increases, whereas the required settling time decreases. Beside that, large number of buffer amplifiers built into a single chip creates power dissipation problem. Consequently, a high driving capability buffer amplifier with low static power consumption is indispensable [1]. In order that the TFT-LCD displays beyond 512 gray levels each color, each gray level is required to be less than 6.4 mV for a 1.2.V full scale. Therefore, the output buffer must have an offset voltage less than ±3.2 mV [2]. There are many works on LCD drivers [1-4]. As reported in [1], [3-5], the static power consumption of a folded-cascode amplifier is larger than that of a telescope-cascode one for more current summing circuits and tail current. Also the maximum efficiency of a folded-cascode amplifier is less than 50 percent [6], and thus has poor driving capability. The offset voltages of the folded-cascode operational amplifiers described in [1], [4], are 10 mV and 12.2 mV, respectively. These

reported offset voltages are too high that will create incorrect activation for gray level above 512. As mentioned in [1,7], a buffer with complementary differential pair is able to deliver larger current and thus have better driving capability. In order to achieve higher driving capability with low static power and low offset voltage, we design a newly developed telescope-cascode based buffer amplifier with complementary differential input stage for low power and high resolution applications. Low offset voltage and high driving capability are attained further by a designed pair of auxiliary driving transistors.

II. CIRCUIT AND OPERATION

The designed buffer amplifier with two complementary differential input amplifiers is shown in Fig.1. The circuit was formed by a common-source push-pull stage, The open-loop amplifier transfer function, can be derived by interrupting the feedback loop in Assuming and yields, in the most general case, the following expression:

$$A_V(s) = A_0 \frac{\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_{P1}}\right)\left(1 + \frac{s}{\omega_{P2}}\right)\left(1 + \frac{s}{\omega_{P3}}\right)}$$

where A0 is the DC open-loop gain expressed by

$$A_0 = g_{m1}R_{o1}g_{m2}R_{o2}$$

while, ω_{P1}, ω_{P2} and ω_{P3} are the frequencies of the three amplifier real poles, which are, respectively, given by

$$\omega_{P1} = \frac{1}{(R_{o2} + R_C)C_L} \approx \frac{1}{R_{o2}C_L}$$
$$\omega_{P2} = \frac{1}{R_{o1}C_{o1}}$$
$$\omega_{P3} = \frac{1}{(R_{o2}||R_C)C_{o3}} \approx \frac{1}{R_C C_{o3}}$$

And ω_Z is the frequency of the left-half plane zero introduced by the compensation resistor R_C, which is given by

$$\omega_Z = \frac{1}{R_C C_L}.$$

simulations are also performed to estimate the amplifier offset voltage for different common-mode input voltages. A mean value of 1.2 mV and a maximum value of 5.6 mV are found, with a standard deviation lower than 800 nV. To further demonstrate the effectiveness of the present out put buffer, and provide a performance comparison other previously adopted solutions, a numeric figure of merit is here introduced for the first time, relying on the main performance parameters of an LCD output buffer. Its basic definition is

$$FOM = \frac{C_L}{T_S \cdot I_{DD}}$$

Mn and Mp, which offers good swing characteristics. In order to increase the driving capability, a pair of auxiliary driving transistors, MAp and MAn, are introduced and controlled by two comparators, nCMP and pCMP. The added comparators are merged with the original differential amplifiers to further reduce the power dissipation. Fig. 1 shows

the detailed circuit of the buffer amplifier. In that, transistors and form the complementary telescope-cascode differential stages. The inputs of these stages are connected in parallel. Each of them drives one half of the common-source push-pull stage, In the figure, forms the biasing current source, while and are two sets of comparators and is the auxiliary driving transistor. Amplifiers without and with auxiliary driving transistors, loading with a 1000pF capacitor. It can be observed in the figure that the charging capability is greatly improved for the latter one. For the settling times being defined as the time required for the output signal reaching within 0.2% of the final voltage, the simulated settling times shown in Fig. for the rising edges of curves A and B, represented for the cases without and with auxiliary driving transistors, are 3.1μs and 0.4 μs, Defining R8A(B) and R9A(B) as the channel resistances of the output transistor and the auxiliary driving transistor respectively, the output response of the rising edge can be expressed where VI and VF are the initial and final values of the output voltage, respectively, and where CL is the load capacitance of the buffer amplifier. The positive slew-rate can then be expressed as Transistors and of the input differential pair are active when Vin reaches the center of the supply voltage. Their biasing currents and VB. We choose longer length for transistor to reduce the channel length modulation and to the systematic offset. For the input differential amplifier, the W/L of is chosen the same value as that of but the aspect ratio of is designed smaller than that of while transistors and are designed to have the same sizes. The currents of and can be expressed as From the above equations, it can be observed that the slew From the above equations, it can be observed that the slew rate can be increased by reducing τp, i.e., reducing the channel resistances of the output stage, R8B and R9B, if load capacitance is constant.
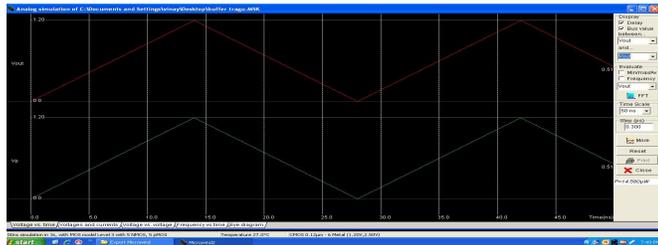
Fig. 1. Block diagram of Amplifier.
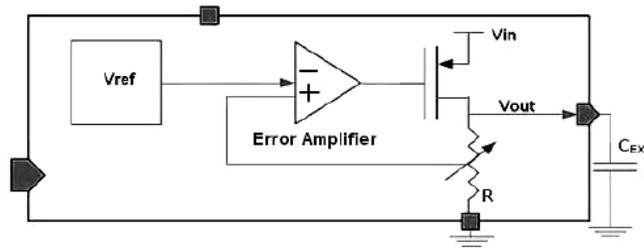
Fig. 2. Circuit Diagram of (Fig.) Buffer Amplifier.
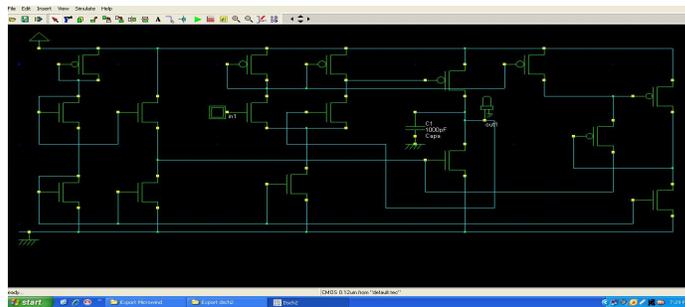
Fig. 3. Output Triangular Wave Buffer Amplifier Buffer.

In a similar way, we can increase the negative slew-rate by reducing the channel resistances of R8A and R9A. Fig. 2 shows the simulated slew rates versus load capacitances (500 pF-5 nF) with 3 V output voltage. Simulated result shows a possible slew rate higher than 18 V/µs for load capacitance less than 1000pF. The simulated offset voltages versus input circuit diagram of (Fig. 2) the proposed buffer amplifier.
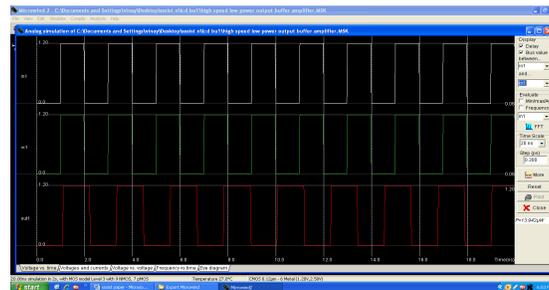
Fig. 4. Output Square Wave Buffer Amplifier.
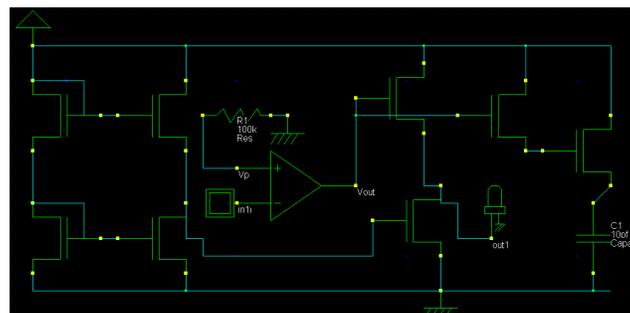
Fig. 5. Circuit Diagram of Buffer Amplifier.

III. EXPERIMENTAL RESULTS

The proposed output buffer amplifier was fabricated using the TSMC 0.6μm CMOS process. Several measurements have been done. The measured static current of the output buffer is 1 μA from a 1.2 V supply voltage. The maximum offset voltage is 2.5 mV, and the slew rate is higher than 18 V/μs for1000pF load capacitance. Fig. 6. shows the measured result of the proposed buffer amplifier under a 50 KHz step input waveform with a 1.2 V amplitude and 1000pF load capacitance shows the measured and simulated settling times for various load capacitances with 1.2 V voltage swing. It is worth mentioned that the settling time is only 1.62 μs even the load capacitance is up to 1000 pF. The die photograph is shown in since the designed circuit is rather neat, the size of the buffer amplifier is only The performance of the proposed buffer amplifier is summarized and compared with the other reported circuits in Fig. 6. It can be observed from the table that the proposed buffer amplifier has a superior performance than that of the other circuits on slew rate, settling time, offset voltage, and static current.
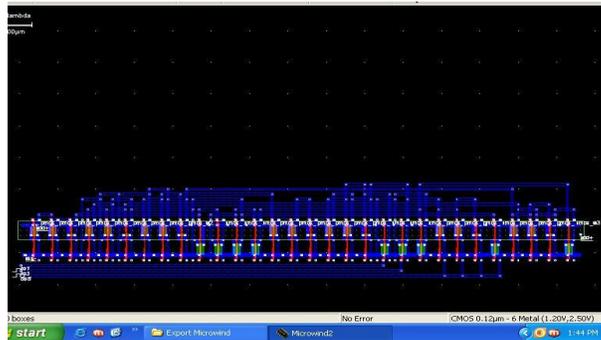
Fig. 6. Die Photograph of the Designed Buffer Amplifier.

IV. CONCLUSION

In this paper, we have designed and demonstrated a high driving capability CMOS buffer amplifier with low static power, and low offset voltage, which is suitable for the source drivers of high resolution LCD with gray levels above 512. The well designed telescope-cascode based buffer amplifier consumes only 1 μA static current and achieves 18 V/μs slew rate for 1000 pF load capacitance. Thus, the buffer amplifier is quite promising for high resolution flat-panel displays that require low static power, high driving capability and high accuracy Buffer amplifier for large -size LCD applications

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